

Fig. 1

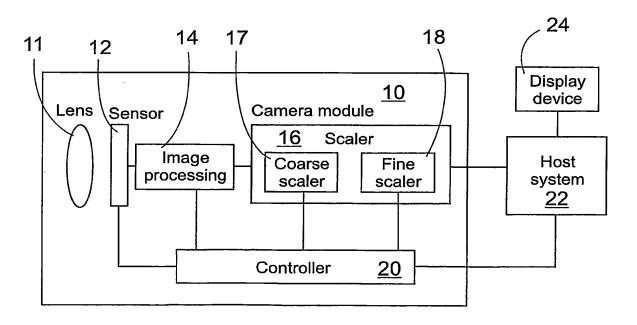


Fig. 2a

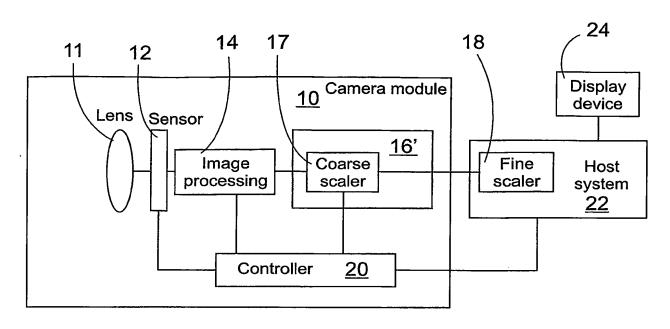
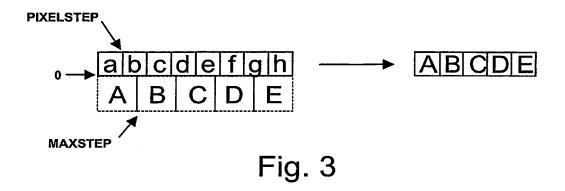


Fig. 2b 17 18 16' 163 162 183 Host system <u>22</u> <u>10</u> 182 CPU Memory Memory CPU Input Input Output < Output unit unit 184 Control Control 164 181 161 165 185 187 167

Fig. 2c



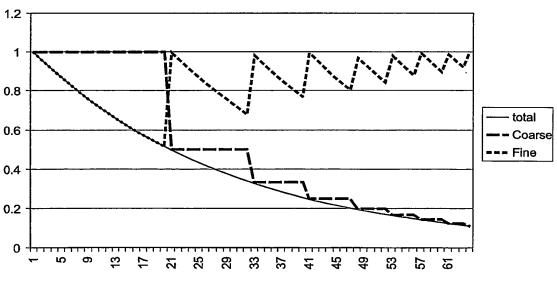


Fig. 4a

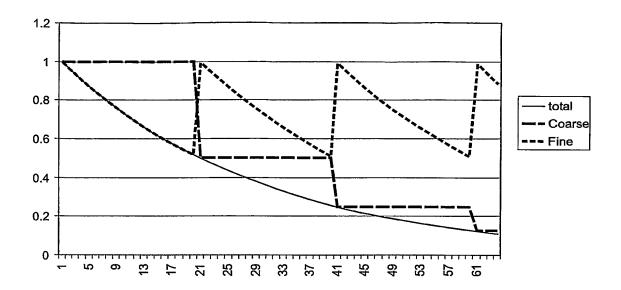


Fig. 4b

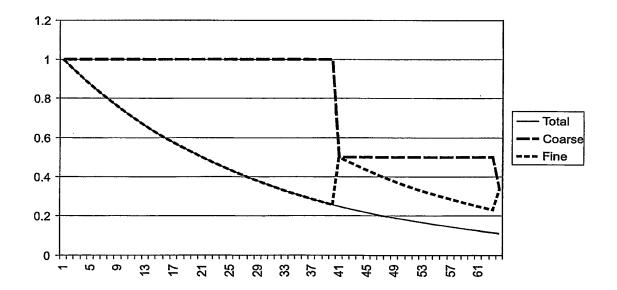


Fig. 4c